

## CLAIMS

1. A video request manager comprising:

a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and

a second state machine for commanding a memory controller to write a second portion of the picture.

2. The video request manager of claim 1, wherein the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion.

3. The video request manager of claim 2, wherein the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention.

4. The video request manager of claim 3, wherein the second state machine commands the memory controller to write the second portion, such that the second portion is written to the memory controller while the memory controller fetches the reference pixels.

5. A circuit for decoding video data, said circuit comprising:

a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator for decoding another portion of the picture; and

a video request manager comprising:

a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and

a second state machine for issuing a command to write a second portion of the picture.

6. The circuit of claim 5, further comprising:

a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

7. The circuit of claim 6, wherein the memory controller further comprises:

an arbiter for causing the memory controller to give priority to the command to fetch the reference pixels.

8. The circuit of claim 6, wherein the memory controller further comprises:

a write buffer for storing the second portion of the picture while fetching the reference pixels.

9. The circuit of claim 8, wherein the memory controller writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels.

10. A method for decoding video data, said method comprising:

calculating at least one address for reference pixels for a first portion of a picture;

decoding another portion of the picture; and

issuing a command to fetch reference pixels for a first portion of a picture; and

issuing a command to write a second portion of the picture.

11. The method of claim 10, wherein issuing the command to write causes a resource contention between the command to fetch reference pixels, and the command to write the second portion.

12. The method of claim 11, wherein the command to fetch reference pixels is given priority during the resource contention.

13. The method of claim 10, further comprising:

fetching the reference pixels after the first state machine issues the command;

loading the second portion of the picture while fetching the reference pixels.

14. The method of claim 10, wherein the first portion comprises a macroblock, and wherein the second portion comprises another macroblock.